A 40/43-Gb/s CDR/DEMUX and MUX Chipset Integrated on a MCM-ceramic with 3R-regeneration functionality

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Abstract —**A second-generation 40/43-Gb/s CDR/DEMUX and MUX chipset in a 120-GHz-ft SiGe technology is presented. While consuming 3.4-W, the fully-integrated CDR/DEMUX provides an electrical sensitivity of less than 40-mVpp at a BER of 10^{-12}, the MUX consumes 2.3-W. Additionally, the integration of the chipset as a 3R-regenerator on a ceramic is demonstrated.**

I. Introduction

While system-suppliers are evaluating 40-Gb/s fiber-optical time-division-multiplexing (TDM) links as next-generation interface technology, mainly for PMD-unaffected short-haul applications, robust chipsets in production-technology are in demand. Two basic electronic functions strongly determine the link performance: the clock and data recovery (CDR) functionality including the demultiplexer (DEMUX) and the multiplexer (MUX) including the clock multiplying unit (CMU), generally known as Serializer-Deserializer (SerDes) chipset. First generation chips or chipsets with a functional subset, e.g. [1, 2], were already presented.

The focus of this work is:

1) Presentation of second generation CDR/DEMUX and MUX chipset with higher level of integration, low power consumption integrated in a 120-GHz-f_T SiGe heterojuntion bipolar technology (HBT). Both devices work with the standard SONET bitrate of roughly 40-Gb/s as well as with increased bitrate of 43-Gb/s for forward-error-correction (FEC) with 7-8% data redundancy.

2) Ceramical integration of the chipset in cascaded manner as a 3R-regenerator in a small-form-factor multi-chip module (MCM) with emphasis on mounting-technique and thermal issues. The ceramic provides retiming, reshaping and reamplification (3R). The specially cascaded application is highly suitable for presenting purposes, whereas in general both chips interact locally separated.

Fig. 1. illustrates the 3R-regenerator embedded in the optical link.

Three possible applications of the device, as shown, are possible. The 3R-regenerator can work as

1) a repeater with the receive-side driven by an optical-to-electrical converter (O/E) as a single photo-diode or together with a trans-impedance-amplifier (TIA) and the transmit-side driving an electrical-to-optical converter (E/O).

2) Secondly, the 3R-regenerator can work as an enhanced receiver with the receive-side driven by an O/E and the transmit-side driving a low-performance electrical receiver.

3) The device can work as an enhanced transmitter with the receive-side driven by a low-performance electrical transmitter and the transmit-side driving an E/O.

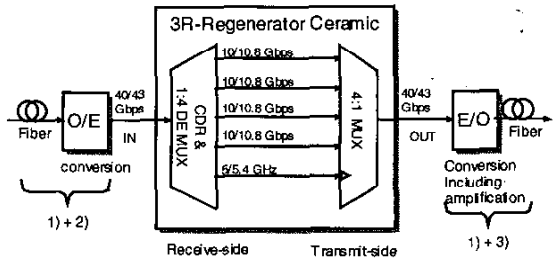

Fig. 1. 3R-regenerator embedded in the optical link

II. Chip Technology

The SerDes-chipset presented in this work was designed in a SiGe HBT production-process with 120-GHz f_T and 100-GHz f_{max} [3]. The process features BiCMOS integration with 0.18u CMOS and bipolar (emitter-width) structure size. Additionally, it provides a five metal stack including a thick metal layer on top. As a standard process option, the low-inductive flip-chip mounting technique is supported, which drastically simplifies and improves device mounting, however, at a minimum of the costs compared to other techniques.

III. CDR/DEMUX

The CDR/DEMUX-IC as part of the chipset is a fully-integrated receiver featuring:

1) the clock and data recovery of the 40/43-Gb/s input
2) 1:4 parallel demultiplexing to 10/10.8-Gb/s streams
3) a 30-dB limiting amplifier at the data input
4) the fully-integrated clock-generation with VCO and orthogonal clock generation via frequency divider and phase-shifter for controlling the decision instant.

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A. Architecture

The architecture and concept of this device mainly is based on [1]. Fig. 2. gives an overview of the architectural blocks. Accordingly, a phase-locked loop (PLL) based approach of the clock recovery with a self-aligned bang-bang-phase detector is employed. The digital phase-detector output signals UPN and DOWNN force the switchable 40/43-GHz VCOs to track to the phase of the input data signal. Similar to [1] the 1:2 DEMUX and the bang-bang phase-detector are combined since the architecture is a half-bit-rate type. Consequently, a four-phase clock at $f_{bitrate}/2$ is mandatory. This clock signals are generated by dividing the switchable 40/43-GHz-VCOs-output-signals in a 2:1 frequency divider. By implementing a phase-shifter, the decision instant can be adjusted with respect to possible signal distortion.

The fully-integrated PLL-filter has a parallel proportional (P) integrating (I) P-I structure. The decoupling of both filter components is most important, since - working at different speeds – the lead-time needs to be minimized to avoid instability of the loop.

As a frequency acquisition aid a frequency-sensitive frequency window detector is implemented which locks to the external 622/672-MHz reference at CI_622M.

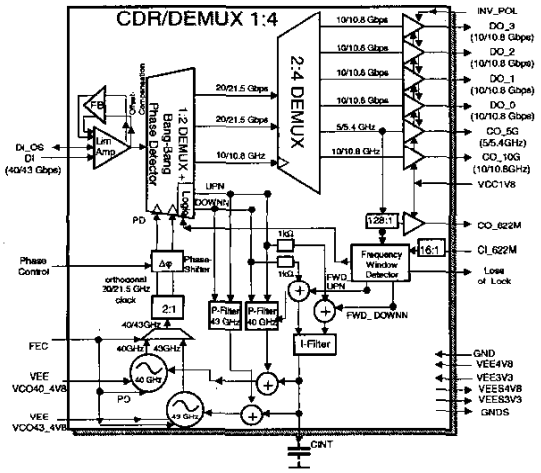

Fig. 2. Architectural overview CDR/DEMUX

The basic circuit concepts at transistor-level used all over in the CDR/DEMUX and MUX are exemplary demonstrated in the integrated limiting amplifier as a typical broadband circuit.

B Implementation - Limiting Amplifier

The limiting amplifier employs cascaded chains of emitter followers (EF), transadmittance stages (TAS) and transimpedance stages (TIS) as indicated in Fig. 3. This is based on the concept of impedance mismatch between succeeding stages [4].

Layout aspects and especially signal interconnects strongly influence the circuit performance at high frequencies. Signal interconnects between current interfaces consisting of TAS and its load - active TIS or passive resistors - are less critical compared placing them between other interfaces [4]. The concept of partitioning into blocks via current interfaces is extensively used in the chipset.

The data input is a 50-Ω input terminated by parallel 70-Ω and 180-Ω resistors while the OS-input allows to force a differential offset to control the threshold (see Fig. 3).

In general, the sensitivity of the CDR is determined by the sensitivity of the limiting amplifier. An input related sensitivity $V_{DI,pp,min}$=17-mVpp for a bit error rate (BER) of 10^{-12} can be calculated via the input equivalent noise voltage $V_{DI,ieqn}$ (simulated to 1.2-mV_{RMS}) similar to [5]:

$$V_{DI,pp,min} \approx 14*V_{DI,ieqn} \approx 14 * 1.2\text{-}mV_{RMS} \approx 17\text{-}mV_{pp} \quad (1)$$

This calculated value of 17-mV_{pp} gives a noise-limited estimation for the actually measured sensitivity in VII.

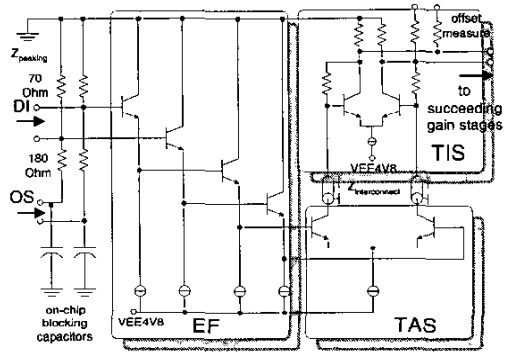

Fig. 3. Circuit diagram of the limiting amplifier (1st gain stage)

IV. MUX

The architecture of the second IC of the 40/43-Gb/s chipset, the 4:1 MUX, is illustrated as part of Fig. 7.

Sub-bit skew between the four 10/10.8-Gb/s input data channels can be compensated in the delay-locked-loop block (DLL).

Synchronization of the two clock domains, namely the 5/5.4-GHz and 20/21.5-GHz input clocks, is performed by a phase frequency detector (PFD). It compares the two clocks and thereby generates a control signal to tune the external 20/21.5-GHz clock signal up/down. The loop filter function within this PLL is integrated as well.

V. PHYSICAL REALIZATION OF THE CHIPSET

Tab. 1 summarizes the power dissipation and the physical die-size of both ICs of the chipset. Both ICs use a

negative -4.8-V supply for all the high-speed-blocks and a -3.3-V supply for the low-speed-parts.

Parameter	Value
CDR/DEMUX: P_{VEE4V8} - -4.8-V supply	4.8-V * 520-mA= 2.5-W
CDR/DEMUX: P_{VEE3V3} -3.3-V supply	3.3-V * 280-mA= 0.9-W
MUX: P_{VEE4V8} - -4.8-V supply	4.8-V * 320-mA= 1.5-W
MUX: P_{VEE3V3} -3.3-V supply	3.3-V * 220-mA= 0.7-W
Chip Area (both)	4.3-mm * 3.2-mm

Tab. 1. Physical realization

The devices' area, as the micrograph of the CDR/DEMUX in Fig. 4 illustrates, is mainly determined by thermal constraints. Since the thermal cooling is performed via the flip-chip-bumps (located between pad and ceramic), a number of 150 flip-chip-bumps yields in a slight increase in temperature of ΔT=15K compared to the ambient temperature for the CDR/DEMUX:

$$\Delta T = R_{th,total} * P_{CDR} = R_{th,single\_flip\text{-}chip\_interconnect}/150 * 3.4W$$

$$= 660K/W / 150 * 3.4W = 14.96K \quad (2)$$

Therefore most of the chip-area is allocated by the flip-chip-bumps, where the majority serves as thermal bumps without electrical purpose.

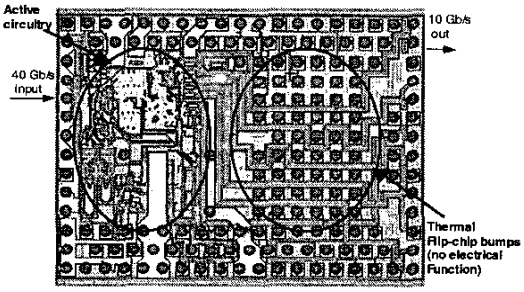

Fig. 4 Micrograph CDR/DEMUX

VI. MODULE OVERVIEW WITH CDR/DEMUX AND MUX AS KEY COMPONENTS

Fig. 7 shows the implementation of the 3R-regenerator ceramic as the cascade of the chipset. For the MUX clock generation three additional ICs, the 40/43-GHz-VCOs and a frequency divider, which are basically building blocks of the CDR/DEMUX, are cermically integrated. Together with the PFD, these ICs are part the transmit PLL.

To maximize the thermal conductivity, AlO_2 forms the base material with a two layer metalisation. The ceramic is glued onto a gold-plated steel package. Small-size GPPO-connectors are used for the differential 40/43-Gb/s I/Os. The photograph of the package is given in Fig. 5.

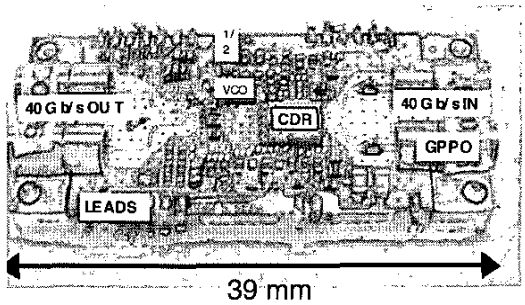

Fig. 5. Packaged regenerator (MUX on backside)

VII. MEASUREMENT RESULTS

The subsequent transmission measurement-results of the SerDes-chipset are performed in the regenerator application. 16 parallel OC48 2^{31}-1 pseudo-random bit sequence signals (PRBS) are multiplexed to one serial 40-Gb/s stream, electrical/optical transformed via an electro-absorptions-modulator (EAM) and fed via fiber to an integrated photodiode (PD) plus transimpedance amplifier (TIA). The single-ended TIA-output is directly connected to the packaged regenerator. Both, PD plus TIA, have an optical/electrical conversion gain of 58.8-V/W.

A Receive part

Fig. 6 shows the corresponding BER-curve as measure of the receiver performance. For a BER of 10^{-12} an optical input power of -5.2-dBm is necessary, resulting in 35.5-mV_{pp} as the measured electrical sensitivity. The theoretically calculated value of 17-mV_{pp} from (1) only considers noise limitations without the effect of ISI and signal shaping.

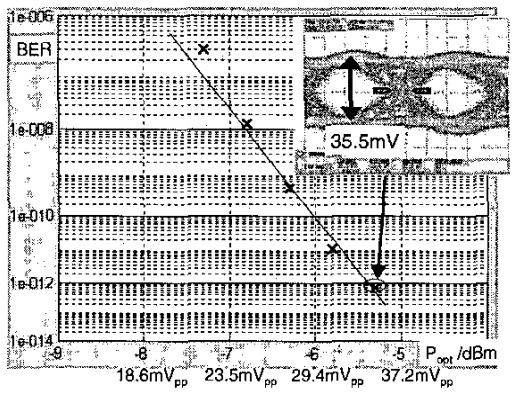

Fig. 6. BER measurement

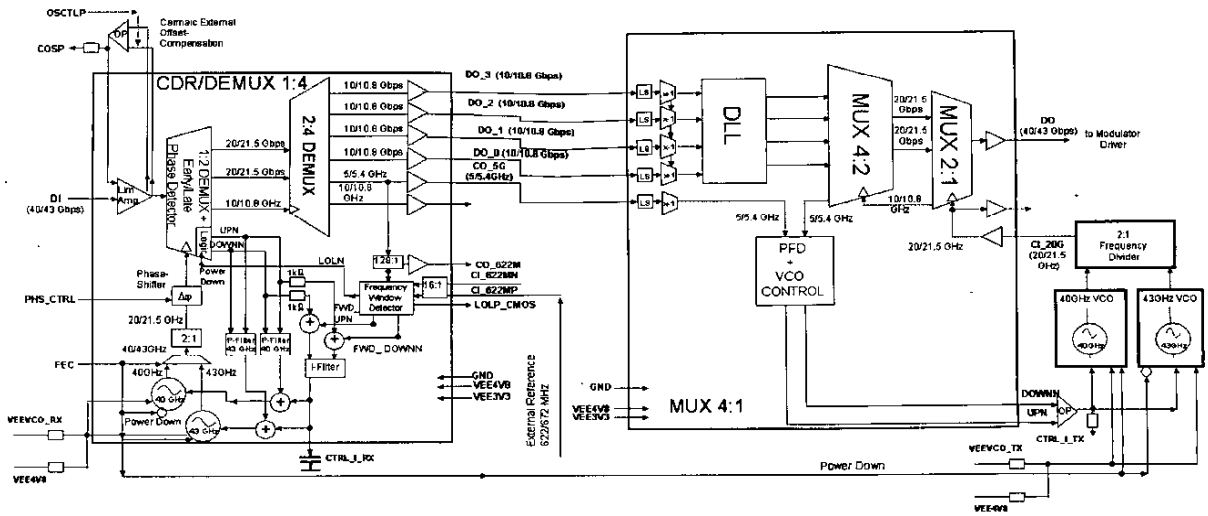

Fig. 7. Architectural overview 3R-regenerator as cascade of CDR/DEMUX and MUX

B. Transmit part

The MUX output eye is given in Fig. 8. A single-ended output swing of 370-mVpp can be observed.

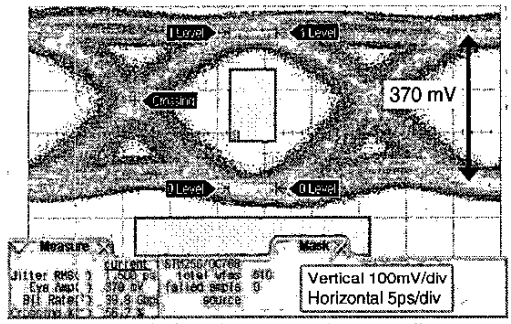

Fig. 8. Single-ended MUX output (mounted)

An additional Power-MUX variant of the MUX has also been evaluated, which provides a 1.25-Vpp single-ended output swing. The promising result of the on-wafer-measurements of this variant with 2^7-1 PRBS is given in Fig. 9.

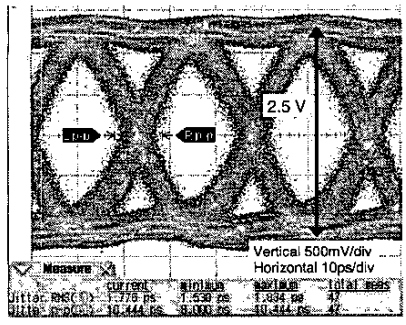

Fig. 9. Differential Power-MUX output (on-wafer)

VIII. CONCLUSION

In this paper the implementation of a second-generation 40/43-Gb/s chipset in a SiGe-HBT production process has been summarized. In addition, the ceramical integration has been successful demonstrated, with optical transmission experiments proved system-relevant functionality.

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